SA2636

3-Phase 600V Gate Driver IC

Description

SA2636 are full bridge drivers to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600 V.

The three independent drivers are controlled at the low-side using CMOS and LSTTL compatible signals, down to 3.3V logic.

SA2636 includes an under-voltage detection unit with hysteresis characteristic and over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down of all six switches. An error signal is provided at the FAULTB open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. Therefore, the resistor R_{RCIN} is optional.

SA2636 typical output current can be given with 300mA for pull-up and 600mA for pull down. Because of system safety reasons a 290ns dead time has been realized. The function of inputs EN and ITRIP can optionally be extended with over-temperature detection, using an external NTC resistor, diodes and resistor network.

Feature

- Fully operate up to 600V
- Gate drive supply range from 10V to 20V
- Built-in dead-time protection
- Shoot-through protection
- Independent Enable/disable input and fault reporting
- Shut down all switches during error conditions
- Adjustable fault clear timing
- 3.3 V/5V/15V input logic compatible
- Tolerant to negative transient voltage, dV/dt immune
- Matched propagation delays for all channels
- Matched dead time
- -40°C to 125°C operating range
- SOP28 Package available

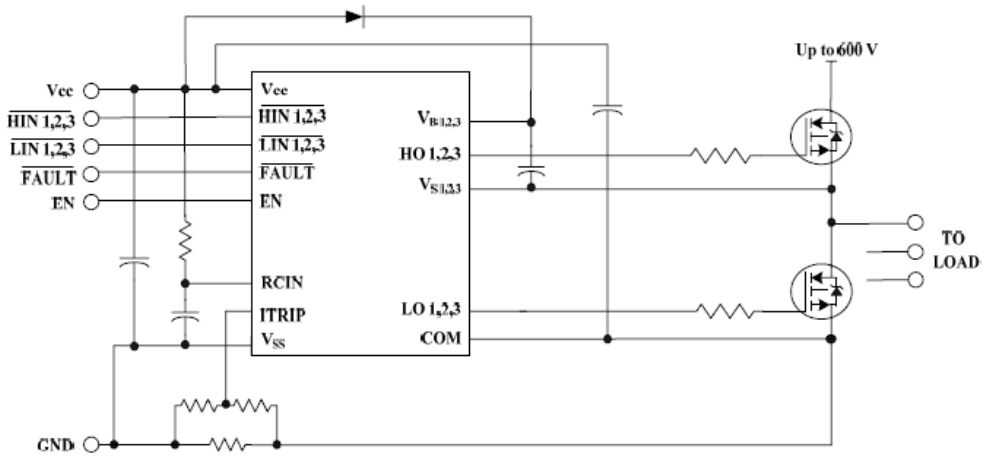
Applications

- Servo drivers
- Industrial inverters
- Appliance motor driver

Device Information

Part No.	Package	Quantity
SA2636	SOP28	1000/Reel

SA2636 Simplified Circuit



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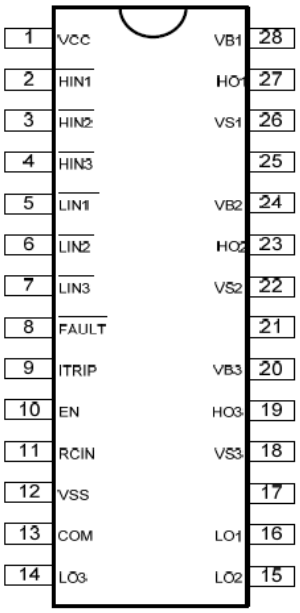
Pin Configuration and Functions



NO.	NAME	TYPE	DESCRIPTION
1	VCC	P	Logic and low-side gate drivers power supply voltage
2,3,4	/HIN1,2,3	I	Logic input for high-side gate driver output (HO), out of phase.
5,6,7	/LIN1,2,3	I	Logic input for low-side gate driver output (LO), out of phase.
8	/FAULT	O	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output.
9	ITRIP	O	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
10	EN	I	Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. No effect on FAULT and not latched.
11	RCIN	I	External RC network input used to define FAULT CLEAR delay, TFLTCLR, approximately equal to R*C. When RCIN>8 V, the FAULT pin goes back into open-drain high-impedance.
12	VSS	P	Logic ground
13	COM	P	Low-side gate drivers return
14,15,16	LO1,2,3	O	Low-side gate driver outputs
17,21,25	NC	NC	No connection
18,22,26	VS1,2,3	P	High-side floating supply return
19,23,27	HO1,2,3	O	High-side gate driver outputs
20,24,28	VB1,2,3	P	High-side floating supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Definition	Symbol	Min	Max	Unit
High side floating supply voltage	V_B	-0.3	700	V
High side offset voltage	V_S	V_B–25	V_B+0.3	
High side floating output voltage	V_{HO}	V_S–0.3	V_B+0.3	
Low side and logic fixed supply voltage	V_{CC}	-0.3	25	
Low side output voltage	V_{LO}	-0.3	V_{CC}+0.3	
Input voltage LIN, HIN, ITRIP, EN	V_{IN}	-0.3	V_{CC}+0.3	
RCIN input voltage	V_{RCIN}	-0.3	V_{CC}+0.3	
FAULTB output voltage	V_{FLT}	-0.3	V_{CC}+0.3	
Allowable offset voltage slew rate	dVs/dt		50	V/ns
Junction temperature	T_J	-40	150	°C
Ambient temperature	T_A	-40	125	
Storage temperature	T_{stg}	-65	150	
Thermal resistance, junction to ambient	θ_{JA}		78	°C/W

Recommended Operating Conditions

The input/output logic-timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The VS offset ratings are tested with all supplies biased at a 15 V differential.

Definition	Symbol	Min	Max	Unit
High side floating supply voltage	V_B	-0.3	600	V
High side offset voltage	V_S	V_B–20	V_B	
High side floating output voltage	V_{HO}	V_S	V_B	
Low side and logic fixed supply voltage	V_{CC}	10	20	
Low side output voltage	V_{LO}	0	V_{CC}	
Input voltage LIN, HIN, ITRIP, EN	V_{IN}	0	V_{CC}	
RCIN input voltage	V_{RCIN}	V_{SS}	V_{CC}	
FAULTB output voltage	V_{FLT}	V_{SS}	V_{CC}	

Static Electrical Characteristics

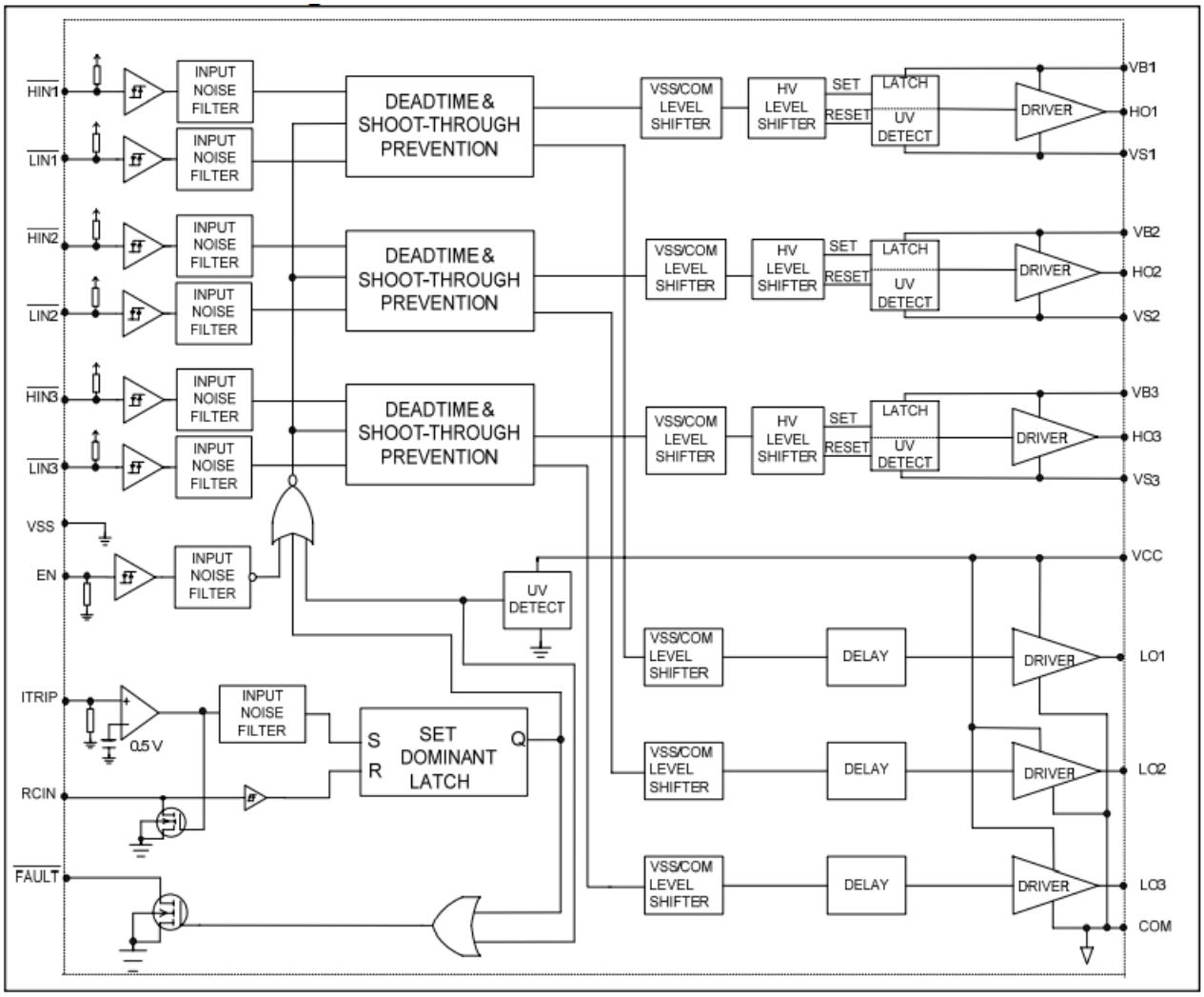
VBIAS (VCC,VBS1,2,3) = 15 V unless otherwise specified. The VIN, VTH, and IIN parameters are referenced to VSS and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The VO and IO parameters are referenced to COM and VS1,2,3 and are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Parameter		Condition	Min.	Typ.	Max.	Unit
Low Side Power Supply						
V_{CC} quiescent current	I_{QVCC}	/HIN1,2,3=0 or 5V /LIN1,2,3=0 or 5V		750	1500	uA
V_{CC} UVLO rising threshold	V_{CCUVR}		8.0	8.9	9.8	V
V_{CC} UVLO falling threshold	V_{CCUVF}		7.3	8.2	9.0	V
V_{CC} UVLO hysterisis	V_{CCUVH}			0.7		V
High Side Floating Power Supply						
High Side V_{BS} quiescent current	I_{QBS}	V_{BS}=15V		60	120	uA
Offset supply leakage current	I_{LK}	V_B=V_S=600V, V_{CC}=0		0.1	50	uA
V_{BS} UVLO rising threshold	V_{BSUVR}		7.7	8.6	9.5	V
V_{BS} UVLO falling threshold	V_{BSUVF}		7.0	7.8	8.7	V
V_{BS} UVLO hysterisis	V_{BSUVH}			0.8		V
Gate Driver Output						
Output Source current	I_{OSRC}	V_O=0, V_{IN}=5V, PW ≤10us		300		mA
Output Sink current	I_{OSIK}	V_O=15V, V_{IN}=0V, PW ≤10us		600		mA
High level output voltage drop	V_{OH}	I_O=20mA		800	1500	mV
Low lvel output voltage drop	V_{OL}	I_O=20mA		300	500	mV
Nagative voltage of output	V_{NG}			-10		V
Logic Input						
Logic"1" input voltage of /HIN1,2,3 and /LIN1,2,3	V_{IH}		2.5			V
Logic"0" input voltage of /HIN1,2,3 and /LIN1,2,3	V_{IL}				0.8	V
Logic"1" input bias current	I_{IH}	V_O=0, V_{IN}=5V		0		uA
Logic"0" input bias current	II_L	V_O=15V, V_{IN}=0V		100	200	uA

Static Electrical Characteristics

Parameter		Condition	Min.	Typ.	Max.	Unit
Shutdown and protection						
RCIN positive going threshold	V_{RCINR}			8.0		V
RCIN hystersis	V_{RCINH}			3.0		V
RCIN pull down MOSFET	R_{RCIN}	I_{SINK}=2mA		30	50	Ω
ITRIP positive going threshold	V_{ITRIPR}		350	450	550	mV
ITRIP hystersis	V_{ITRIPH}		40	70		mV
EN rising threshold	V_{ENR}		2.5			V
EN falling threshold	V_{ENF}				0.8	V
High enable input bias current	I_{ENH}			60	120	uA
Low enable input bias current	I_{ENL}			0		uA
/FAULT on resistance	R_{ON_FLT}	I_{SINK}=2mA		30	50	Ω
Timing						
Turn on propagation delay	t_{ON}	V_{CC}=15V, V_{BS}=15V, C_L=1nF		425	550	ns
Turn off propagation delay	t_{OFF}			425	550	ns
Turn on Rise time	t_R			125	190	ns
Turn on Fall time	t_F			50	75	ns
Input filter time	t_{FLTIN}			350		ns
Enable low to output shutdown propagation delay	t_{EN}			450	600	ns
ITRIP to output shutdown propagation delay	t_{ITRIP}			750	1000	ns
ITRIP blanking time	t_{BL}			350		ns
ITRIP to /FLAUT propagation dealy	t_{FLT}			650	900	ns
FAULT clear time RCIN	t_{FLTCLR}	R=2MΩ,C=1nF		1.75	2.0	ms
Dead time	DT		200	290	380	ns
Matching delay ON and OFF	MT			20	75	ns
Output pulse width matching	PM			40	75	ns

Function Block Diagram



Timing Diagram

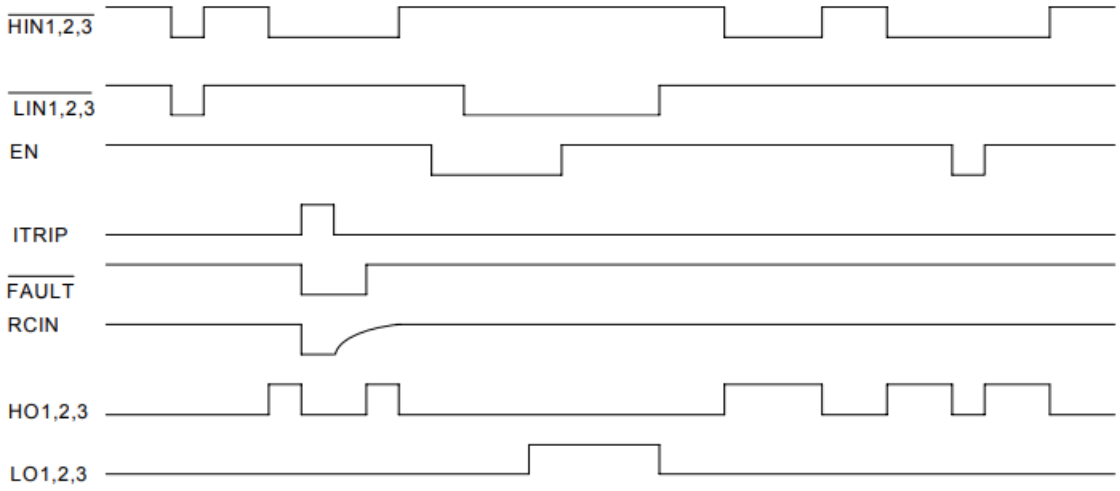


Fig1. Input/Output Timing Diagram

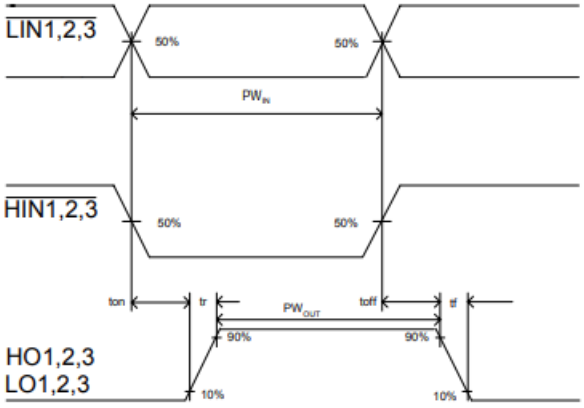


Fig2. Switching time

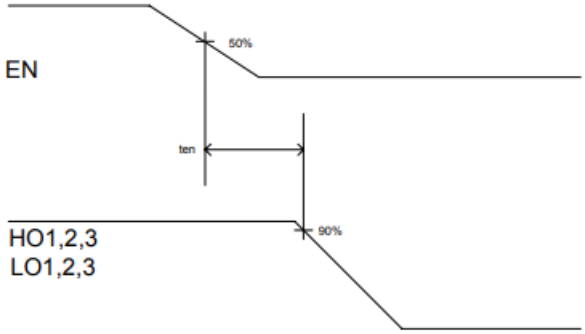


Fig3. Output Enable timing

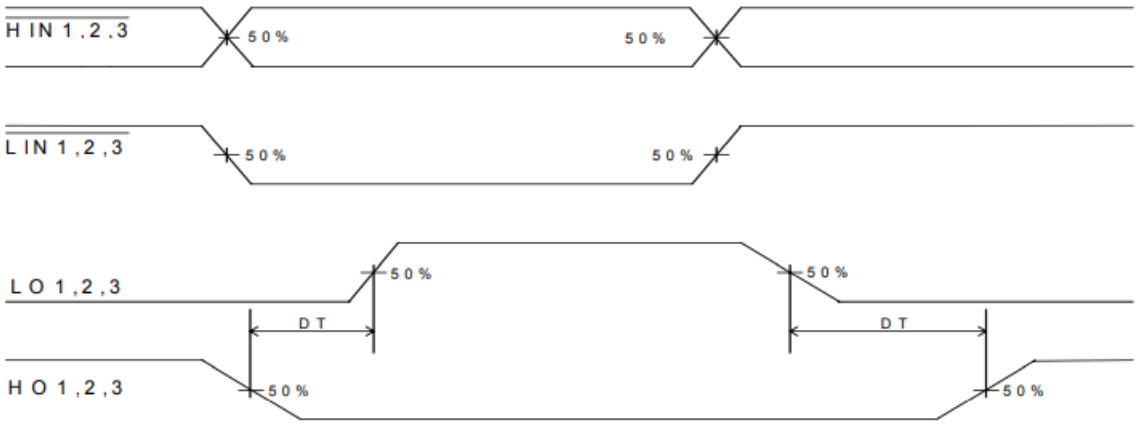


Fig4. Internal Deadtime timing

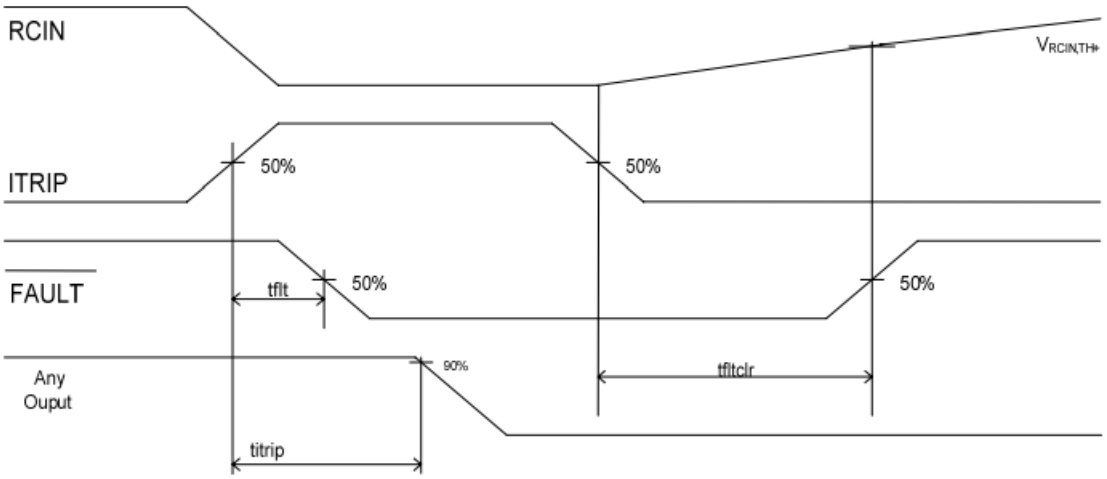


Fig5. IRTIP/RCIN timing

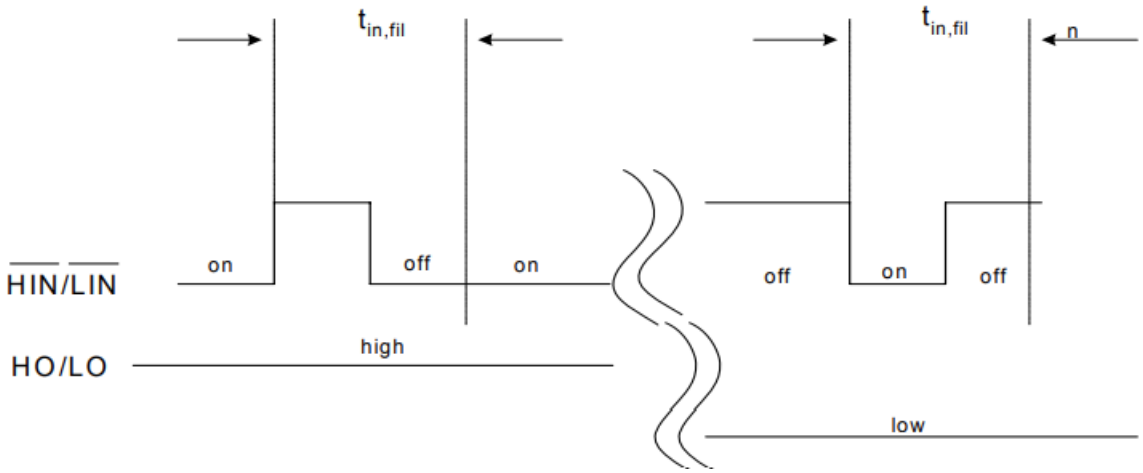
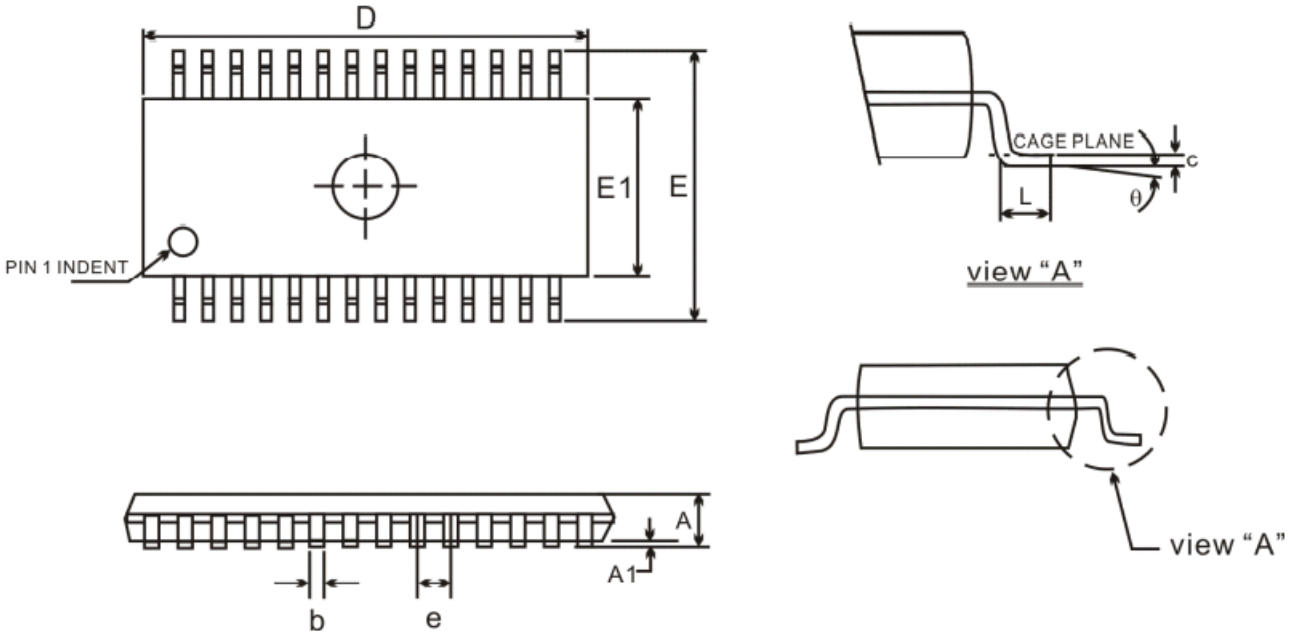


Fig6. Input Filter timing

Package Information

SOP28



Symbol	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	0.30
b	0.31	-	0.51
c	0.20	-	0.33
e		1.27 BSC.	
D		17.90 BSC.	
E		10.30 BSC.	
E1		7.50 BSC.	
L	0.38	-	1.27
θ	0°	-	8°

Notes:
1. All controlling dimensions are in millimeter.
2. Refer to JEDEC MS-013 AD.

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